Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in this application.

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

a borderless logic array comprising repeating cores; area I/Os, wherein at least one of said area I/Os is located in said semiconductor device such that some of said repeating cores are placed adjacent to two opposite sides of the area I/O; ~~and wherein said logic array comprises a repeating core, and~~ wherein at least one of said area I/Os is a configurable I/O, and wherein said configurable I/O comprises at least one metal layer that is the same for all I/O configurations.

2. (Canceled)

3. (Currently Amended) A semiconductor wafer comprising:

a borderless logic array, wherein said borderless logic array comprises a repeating module containing logic cells and I/O cells and a redistribution layer for redistributing at least some of said I/O cells' connections to pads used in packaging, wherein at least one of said I/O cells comprises an area I/O having logic cells adjacent to opposite sides of the area I/O.

4. (Original) A semiconductor wafer according to claim 3, wherein said I/O cells are arranged in spaced parallel lines.

5. (Original) A semiconductor wafer according to claim 4, wherein spaced parallel lines are spaced at least 0.2 mm apart but less than 3 mm apart.

6. (Original) A semiconductor wafer according to claim 3, wherein said repeating module comprises at least two metal layers.

7. (Original) A semiconductor wafer according to claim 6, wherein at least one of said metal layers comprises a repeating pattern.

8. (Original) A semiconductor wafer according to claim 6, wherein each of said metal layers comprises a repeating pattern.

9. (Currently Amended) A semiconductor wafer according to claim 6, wherein additional custom layers are arranged to define a specific die size on said semiconductor wafer.

10. (Currently Amended) A semiconductor wafer according to claim 6, wherein additional custom layers are arranged to define at least two different die sizes on said semiconductor wafer.

11.-13. (Canceled)

14. (Previously Presented) A semiconductor device according to claim 1, wherein said configurable I/O comprises:

at least two electronic components; and

multiple possible connections among said electronic components, wherein at least one custom via layer is used to complete at least one of said possible connections to configure said configurable I/O.

15. (Previously Presented) A semiconductor wafer according to claim 3, wherein at least one of said I/O cells comprises:

at least two electronic components; and

multiple possible connections among said electronic components, wherein at least one custom via layer is used to complete at least one of said possible connections to configure at least one of said I/O cells.

16. (Currently Amended) A semiconductor device comprising:

a borderless logic array comprising repeating cores; area I/Os, wherein at least one of said area I/Os is located in said semiconductor device such that some of said repeating cores are placed adjacent to two opposite sides of the area I/O; and wherein said logic array comprises a repeating core and a redistribution layer for redistributing at least some of said area I/O connections to pads used in packaging.

17. (Currently Amended) A semiconductor device comprising:

a borderless logic array; area I/Os, wherein at least one of said area I/Os is located in said semiconductor device such that there is logic adjacent to two opposite sides of the area I/O; and wherein at least one of said area I/Os is a configurable I/O, and a redistribution layer for redistributing at least some of said area I/O connections to pads used in packaging.

18. (Currently Amended) A ~~semiconductor~~ logic array device comprising:

a borderless logic array; area I/Os, wherein at least one of said area I/Os is located in said semiconductor device such that there is logic adjacent to two opposite sides of the area I/O; and wherein at least one of said area I/Os is a configurable I/O, and wherein said configurable I/O comprises at least one metal layer that is the same for all I/O configurations.

19. (Previously Presented) A ~~semiconductor wafer~~ logic array device according to claim 18, wherein said configurable I/O further comprises:

at least two electronic components; and

multiple possible connections among said electronic components, wherein a custom via layer is used to complete at least one of said possible connections to configure said configurable I/O.

20. (New) A semiconductor device according to claim 1, wherein some of said area I/Os are arranged in spaced parallel lines.

21. (New) A semiconductor device comprising:

a continuous logic array comprising repeating cores; area I/Os, wherein at least one of said area I/Os is located in said semiconductor device such that some of said repeating cores are placed adjacent to two opposite sides of the area I/O;

wherein at least one of said area I/Os is a configurable I/O, and wherein said configurable I/O comprises at least two metal layers that are the same for all I/O configurations.

22. (New) A semiconductor device comprising:

area I/Os, where at least one of said area I/Os is located in said semiconductor device such that logic is placed adjacent to two opposite sides of the area I/O;

wherein at least one of said area I/Os is a configurable I/O, and wherein said configurable I/O comprises at least two metal layers that are the same for all I/O configurations.

23. (New) A semiconductor wafer comprising:

a continuous logic array, wherein said continuous logic array comprises a repeating module containing logic cells and I/O cells and a redistribution layer for redistributing at least some of said I/O cells' connections to pads used in packaging;

wherein at least one of said I/O cells comprises area I/O having logic cells adjacent to opposite sides of the area I/O.

24. (New) A semiconductor wafer comprising:

a logic array, said logic array comprising a repeating module containing logic cells and I/O cells and a redistribution layer for redistributing at least some of said I/O cells' connections to pads used in packaging;

wherein at least one of said I/O cells comprises an area I/O having logic cells adjacent to opposite sides of the area I/O.

25. (New) A semiconductor wafer according to claim 24, wherein said I/O cells are arranged in spaced parallel lines.

26. (New) A semiconductor wafer according to claim 25, wherein said spaced parallel lines are spaced at least 0.2 mm apart but less than 3 mm apart.

27. (New) A semiconductor device according to claim 24, wherein said repeating module comprises at least two metal layers, wherein at least one of said two metal layers comprises a repeating pattern.